	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L6	100	(press adj fit$4 or weld) same lead adj frame$1 and (chip or ic or die) and (encapsulat$4 or resin or epoxy)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/03/21 12:11
2	BRS	L7	463	(press adj fit$4 or weld$4) same lead adj frame$1 and (chip or ic or die) and (encapsulat$4 or resin or epoxy)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/03/21 12:33
3	BRS	L8	0	kr-0027651-$.did.	EPO; JPO; DERWENT	2002/03/21 12:33
4	BRS	L9	0	kr-27651-$.did.	EPO; JPO; DERWENT	2002/03/21 12:35
5	BRS	L10	205	first adj lead adj frame same second adj lead adj frame and (chip or die or ic)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/03/21 12:37

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	10	(ic or chip or die) same source same gate same (bump$1 or ball$1) and lead near2 frame and (epoxy or resin or encapsulant or mold$4 near3 body)	USPAT; EPO; JPO; DERWENT; IBM TDB	2002/03/10 15:56
2	BRS	L2	332	plurality near5 lead near2 frame and (bump$1 or ball$1) with (die or chip or ic)	USPAT; EPO; JPO; DERWENT; IBM TDB	2002/03/10 16:39
3	IS&R	L20	0	("438/123 and (bump$1 or ball$1)").CCLS.	USPAT	2002/03/10 16:59
4	BRS	L21	381	438/123 and (bump$1 or ball$1)	USPAT	2002/03/10 16:59
5	BRS	L22	116	438/123 and (bump$1 or ball$1) and (source or gate)	USPAT	2002/03/10 17:09
6	BRS	L38	283	438/124 and lead near2 frame	USPAT	2002/03/10 17:09
7	BRS	L39	27	438/124 and lead near2 frame same (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:10
8	BRS	L40	91	438/124 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:13
9	BRS	L41	68	438/126 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:14
10	BRS	L42	80	438/127 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:16
11	BRS	L43	315	257/666 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:22
12	BRS	L44	169	257/668 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:25

	Type	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L45	60	257/672 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:26
14	BRS	L46	233	257/676 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:29
15	BRS	L47	27	438/110 and lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	USPAT	2002/03/10 17:37
16	BRS	L48	535	lead near2 frame and (chip or die or ic) with (bump$1 or ball$1)	EPO; JPO; DERWENT; IBM TDB	2002/03/10 17:38

CLIPPEDIMAGE= JP405206354A
PAT-NO: JP405206354A
DOCUMENT-IDENTIFIER: JP 05206354 A
TITLE: SEMICONDUCTOR PRESSURE SENSOR AND ITS MANUFACTURE

PUBN-DATE: August 13, 1993

INVENTOR-INFORMATION:
NAME
ISHIBASHI, KIYOSHI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
MITSUBISHI ELECTRIC CORP	N/A

APPL-NO: JP04010825
APPL-DATE: January 24, 1992

INT-CL_(IPC): H01L023/50; G01L019/14 ; H01L021/52 ; H01L029/84
US-CL-CURRENT: 257/676

ABSTRACT:
PURPOSE: To prevent the loop deformation and the break of a gold wire, which connects the semiconductor pressure sensor chipmounted on a die pad with the lead of a lead frame, by elevating the rigidity of a die pad part and the rigidity of lead part at large.

CONSTITUTION: The lead frame 200 of a semiconductor pressure sensor is made by making the first lead frame 210, which has a twin-bun structure of die pad part 211, and the second lead frame 220 equipped with a lead 21 separately, and laying these two leads on top of the other and coupling them by spot welding 48 thereby uniting them, thus the rigidity of the die pad part 211 and the rigidity of the lead frame at large are elevated.

DERWENT-ACC-NO: 2001-473541
DERWENT-WEEK: 200151

TITLE: Semiconductor package and manufacturing method thereof

INVENTOR: KIM, B M

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 1999KR-0027651 (July 9, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001009329 A	February 5, 2001	N/A	001	H01L 023/48

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001009329A	N/A	1999KR-0027651	July 9, 1999

INT-CL_(IPC): H01L023/48

ABSTRACTED-PUB-NO: KR2001009329A
BASIC-ABSTRACT: NOVELTY - A semiconductor package is provided to minimize
package defects caused by a defective contact between lead frames, by adhering
the lead frames by a spot welding using a laser or high voltage after aligning
the lead frames.

DETAILED DESCRIPTION - A semiconductor package comprises the first lead frame,
the second lead frame, a semiconductor chip(400), a wire and a molding resin.
The first lead frame further comprises a conductive strip body, inner
leads(120) and outer leads(130). The inner leads are established inside a

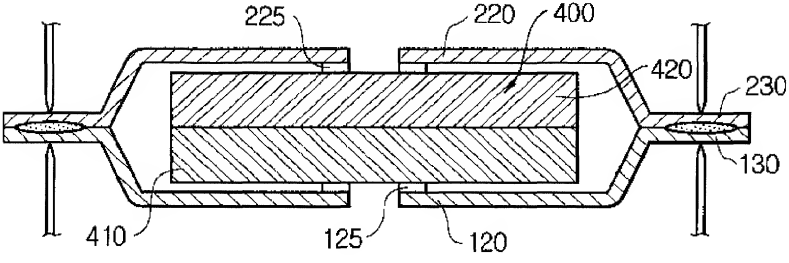
plurality of molding regions formed in the strip body. The outer leads are
formed outside the molding region. The second lead frame further comprises a
conductive strip body, inner leads(220) and connection leads(230). The inner
leads are established inside a plurality of molding regions formed in the strip
body. The connection leads are formed inside the molding region and connected
to the outer lead by thermal resistance generated by a thermal resistance
generating unit. The semiconductor chip is adhered to the inner lead of the
first and second lead frames while being insulated. The wire electrically
connects the inner lead with the semiconductor chip. The molding resin
encapsulates the first and second lead frames, the semiconductor chip and the
wire.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS:
SEMICONDUCTOR PACKAGE MANUFACTURE METHOD

DERWENT-CLASS: U11

EPI-CODES: U11-D03A;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DERWENT-ACC-NO: 2002-088131
DERWENT-WEEK: 200212

TITLE: Method for manufacturing dual die package

INVENTOR: KWAK, M G

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 2000KR-0003957 (January 27, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001076670 A	August 16, 2001	N/A	001	H01L 023/28

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001076670A	N/A	2000KR-0003957	January 27, 2000

INT-CL_(IPC): H01L023/28

ABSTRACTED-PUB-NO: KR2001076670A
BASIC-ABSTRACT: NOVELTY - A method for manufacturing a dual die package is
provided to proceed the coupling process of the leads of the first lead frame
and the second lead from with a conductive film to simplify the manufacturing
process.

DETAILED DESCRIPTION - The dual die package manufacturing method includes
following steps. At first, the first lead frame(40) including the first lead
which includes the first coupling member and the first junction member and the
first damper. At second, the second lead frame including the second lead which
includes the second coupling member and the second junction

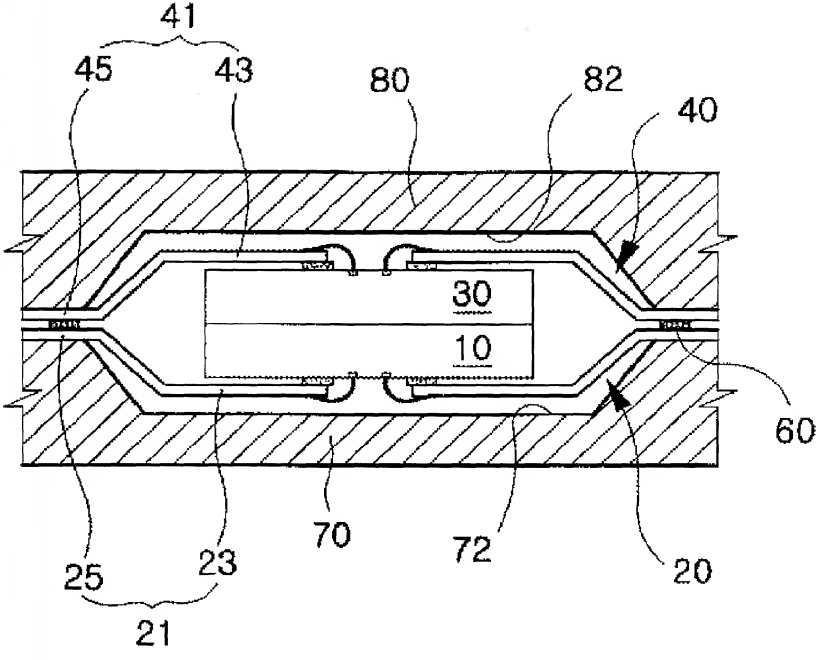
member and the
second damper. At third, the first and the second lead frames are coupled with
each other by applying conductive film between them. At last, a resin is
filled to seal a region where the first and the second semiconductor chips are
implemented to form a package body. The first coupling member is located on an
active region of the first semiconductor chip. The first damper which is
formed in a direction penetrating the first junction member in perpendicular.
The second damper which is formed in a direction penetrating the second
junction member in perpendicular.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS:
METHOD MANUFACTURE DUAL DIE PACKAGE

DERWENT-CLASS: U11

EPI-CODES: U11-E02A1;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DERWENT-ACC-NO: 2001-473362
DERWENT-WEEK: 200151

TITLE: Semiconductor package and manufacturing method thereof

INVENTOR: CHOI, H G; KWAK, M G

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 1999KR-0026832 (July 5, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001008815 A	February 5, 2001	N/A	001	H01L 023/31

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001008815A	N/A	1999KR-0026832	July 5, 1999

INT-CL_(IPC): H01L023/31

ABSTRACTED-PUB-NO: KR2001008815A
BASIC-ABSTRACT: NOVELTY - A semiconductor package is provided to necessitate no additional process for adhering lead frames, by molding at least two lead frames while adhering the lead frames.

DETAILED DESCRIPTION - A semiconductor package comprises the first lead frame(30), the second lead frame(40) and a molding resin(70). The first lead frame includes an inner lead(33) and an outer lead(35). The inner lead is connected to a semiconductor chip(20) by a wire, established inside a molding region with reference to the molding region. The outer lead is protruded by a

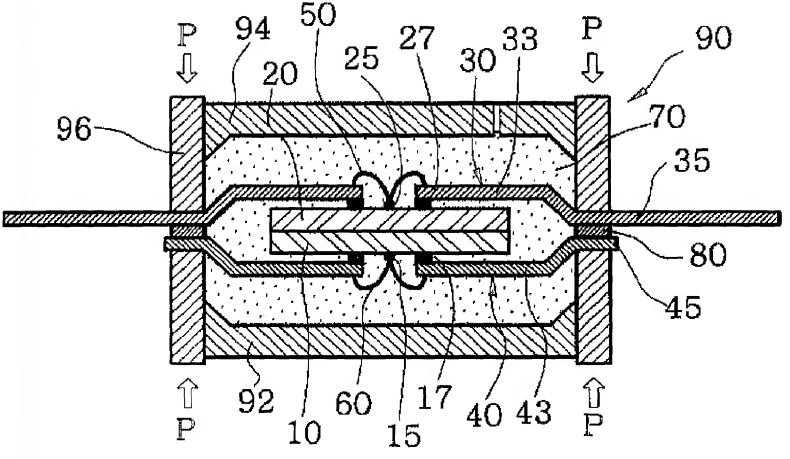
predetermined length to the exterior of the molding region from the inner lead
with reference to the molding region. The second lead frame includes an inner
lead(43) and an outer lead(45). The inner lead is connected to a semiconductor
chip by a wire, established inside a molding region with reference to the
molding region. The connection lead is protruded by a predetermined length to
the exterior of the molding region from the inner lead with reference to the
molding region. The molding resin encapsulates the first and second lead
frames. A metal having a melting point lower than that of Ag is established on
either one of a side of the outer lead or a side of the connection lead
opposite to the side of the outer lead.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS:
SEMICONDUCTOR PACKAGE MANUFACTURE METHOD

DERWENT-CLASS: U11

EPI-CODES: U11-E02A2;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CLIPPEDIMAGE= JP406140548A
PAT-NO: JP406140548A
DOCUMENT-IDENTIFIER: JP 06140548 A
TITLE: RESIN-SEALED SEMICONDUCTOR DEVICE

PUBN-DATE: May 20, 1994

INVENTOR-INFORMATION:
NAME
WATANABE, TOSHIYA

ASSIGNEE-INFORMATION:

NAME	COUNTRY
TOSHIBA CORP	N/A

APPL-NO: JP04288561
APPL-DATE: October 27, 1992

INT-CL_(IPC): H01L023/50; H01L023/28
US-CL-CURRENT: 438/FOR.380,29/827 ,174/52.3

ABSTRACT:
PURPOSE: To realize the low resistance value and to eliminate distortion
(warping) in the final shape.

CONSTITUTION: A first lead frame A has an island 21 for mounting a
semiconductor chip 24. One main surface of the island 21 at the opposite side
of the side, on which the semiconductor chip 24 is mounted, is exposed from a
resin body. A second lead frame B has a distortion preventing member 26 having
the approximately same shape as the island of the first lead frame. One main
surface of the distortion preventing member 26 at the opposite side of the side
facing the island is exposed from the resin bode. This semiconductor device is
constituted in this way.

CLIPPEDIMAGE= JP411312781A
PAT-NO: JP411312781A
DOCUMENT-IDENTIFIER: JP 11312781 A
TITLE: BRIDGE TYPE SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUBN-DATE: November 9, 1999

INVENTOR-INFORMATION:

NAME	COUNTRY
FURUSATO, KOJI	N/A
SASAKI, MITSUMASA	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SHINDENGEN ELECTRIC MFG CO LTD	N/A

APPL-NO: JP10134499
APPL-DATE: April 28, 1998

INT-CL_(IPC): H01L025/07

ABSTRACT:
PROBLEM TO BE SOLVED: To improve productivity by holding a semiconductor chip between two lead frames, to which units in bridge units are connected continuously in the X and Y directions and which have the same or approximately the same shape, and soldering the semiconductor chip.

SOLUTION: A first lead frame, in which solder, etc., are printed beforehand onto die pad sections, is placed on a jig, etc., and diode chips D2, D3 and D1, D4 are incorporated into the die pad sections 1a, 2a while polarity is made to differ respectively. A second lead frame is put on so that the die pad sections 3a, 4a of the second lead frame having the same shape or approximately the same shape as the first lead frame are orthogonally crossed with the die

pad sections 1a, 2a of the first lead frame. Since a bridge circuit is formed under the state, the bridge circuit is joined and unified by soldering by heating. Accordingly, a plurality of the bridge type semiconductor devices can be assembled simultaneously only by the semiconductor chip and solder and the two lead frames having approximately the same shape, and productivity is improved.

DERWENT-ACC-NO: 1996-271012
DERWENT-WEEK: 199628

TITLE: Resin sealed semiconductor device with surge absorption module mfg
method - involves sealing of area surrounding semiconductor element pellet by
resin and then performing tie bar cut and frame tab cut

PATENT-ASSIGNEE: FUJI ELECTRIC CO LTD[FJIE]

PRIORITY-DATA: 1993JP-0309962 (December 10, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 07221236 A	August 18, 1995	N/A	006	H01L 023/48

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP07221236A	N/A	1994JP-0305767	December 9, 1994

INT-CL_(IPC): H01L023/48

ABSTRACTED-PUB-NO: JP07221236A
BASIC-ABSTRACT: The method uses three substrate support bodies (Sa-Sc). An
external lead (6), a tie bar (9b) on a first lead frame (9), a connection
element (7), a table (10a) and a second lead frame (10) form a pattern on a tie
bar (10b).

When a set of semiconductor element pellet (4a-4c) are inserted and the first
and second lead frame are placed on top of the main side, the semiconductor
element pellets are connected to the substrate support bodies through die
bonding. The area surrounding the semiconductor pellet, substrate support body

connection element and external lead are sealed by a resin (8). A tie bar cut
and a tap cut are provided and the resin sealed semiconductor device is thus
assembled.

ADVANTAGE - Increases production efficiency. Increases reliability of product.
Provides surge absorption modules.

CHOSEN-DRAWING: Dwg.1/6

TITLE-TERMS:
RESIN SEAL SEMICONDUCTOR DEVICE SURGE ABSORB MODULE MANUFACTURE METHOD SEAL AREA SURROUND SEMICONDUCTOR ELEMENT PELLET RESIN PERFORMANCE TIE BAR CUT FRAME TAB CUT

DERWENT-CLASS: U11

EPI-CODES: U11-D01B3; U11-D03A1A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1996-227754

CLIPPEDIMAGE= JP02000133676A
PAT-NO: JP02000133676A
DOCUMENT-IDENTIFIER: JP 2000133676 A
TITLE: SEMICONDUCTOR DEVICE

PUBN-DATE: May 12, 2000

INVENTOR-INFORMATION:

NAME	COUNTRY
TANAKA, KUNINOBU	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SONY CORP	N/A

APPL-NO: JP10304930
APPL-DATE: October 27, 1998

INT-CL_(IPC): H01L021/60; H01L023/50

ABSTRACT:
PROBLEM TO BE SOLVED: To provide a semiconductor device which can exhibit a small high-frequency loss, good thermal dissipation and grounding from its rear side, can increase its reliability of connection of a junction between chip electrodes and a substrate pattern, and can be manufactured inexpensively while preventing increase of the number of its manufacturing steps and use of expensive material.

SOLUTION: The semiconductor device includes a semiconductor integrated circuit chip 1 having bumps 2 formed on electrode pads, a first lead frame 3 having external leads 5 formed integrally to a die pad 4, and a second lead frame 6 having inner leads 7 at their tips joined directly to the bumps 2 of the electrode pads and having external leads 8 extended from the inner leads 7. The chip 1 is joined to the die pad 4 of the first lead

frame 3 and the bumps 2
of the electrode pads are joined to the tip ends of the
inner leads 7 of the
second lead frame 6.